Unified Gated Flip-Flops for Reducing the Clocking Power in Register Circuits

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**Background and motivation of our study**

- Large amount of power is dissipated in register circuits
  - Around 40% of the total power in a microprocessor
- Clocking power is dominant in the register circuits
  - More than 80% of the power is due to clock signal transition

**Previous Work**

- Gated flip-flop
  - Clock supply is stopped if data is not updated
- Downside of the gated flip-flop
  - Large delay, area and power overheads

**Our Approach**

- Unify Multiple Gated FFs
  - Reduces internal clocking power
  - Reduces area overhead in gating circuits

**Test Chip Implementation**

**Evaluation using MPU**

- Target Processor
  - Media embedded processor developed by Toshiba
  - RISC type processor with five pipelines
- Comparison
  - CLK Gating: conventional clock gating is applied
  - CONV GFF: conventional gated FFs [4] are used
  - UGFF: unified gated FFs (i.e., ours) are used

**Power Estimation Results**

- The power consumption can be reduced by 25% on average and by 33% at the best case